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Speech processor design for cochlear implants.

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Summary: In this paper, a DFT based speech processor model is developed for the evaluation of different parameters associated with the design of external processor used in a typical cochlear implant system. The key design parameters chosen for investigation in the present work are the bit precisions required at different stages, the impact of increasing the number of channels or stimulant electrodes, the impact of errors in the frequency and amplitude stimulated by individual electrodes. Detailed simulations are first carried out in MATLAB to identify acceptable values for the various design parameters. The design is then mapped on to an FPGA to identify the gate level complexity involved in realizing the processor. The result shows that electrode misplacement (frequency error) can be easily rectified by varying accordingly the channel center frequencies chosen in the external processor. The results presented show that 12-bit precision for formant frequency channels and 8-bit precision for the other channels are adequate to ensure that the normalized Mean Square Error (MSE) is less than 5%. In case of misplaced electrodes, it is shown that allowing for tunability of center frequency of each channel in steps of 10Hz results in the performance improvement by nearly 70% in terms of MSE.

Keywords: cochlear implant (CI); speech processor; continuous interleaved sampling (CIS) algorithm; DFT; acoustic stimulation
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