Le, Qianqi; Yang, Guowu; Hung, William N.N.; Song, Xiaoyu; Zhang, Xinpeng
Pareto optimal mapping for tile-based network-on-chip under reliability constraints.

Summary: Mapping for network-on-chip (NoC) is one of the key steps of NoC design. To improve the performance and reliability of NoC architectures, we present a comprehensive optimization algorithm with multiple objectives. We propose to find the Pareto optimal solutions, rather than a single solution usually obtained through scalarization, e.g. weighting the objective functions. In order to meet the NoC mapping requests and strengthen the capability of searching solutions, the standard particle swarm optimization (PSO) algorithm is improved and a fault-tolerant routing is proposed. These methods help to solve the tradeoff between high performance and system reliability. We present a mathematical analysis of the convergence of the improved algorithms, and prove sufficient conditions of convergence. The improved algorithms are implemented on the Embedded Systems Synthesis Benchmarks Suite (E3S). Experimental results show our algorithms achieve high performance and reliability compared with the standard PSO.

Keywords: optimization algorithm; network-on-chip; mapping; particle swarm optimization; reliability
doi:10.1080/00207160.2014.892073